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PATENT ABSTRACTS OF JAPAN

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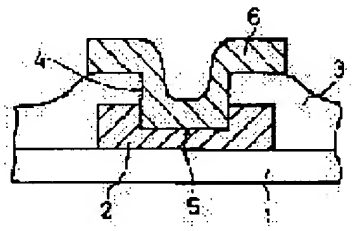
(71)Applicant : **FUJITSU LTD**
(72)Inventor : **OTSUKA TOSHIYUKI**
KANAZAWA MASAO

(54) SEMICONDUCTOR DEVICE AND ITS PRODUCTION

(57)Abstract:
PURPOSE: To provide a semiconductor which has a multi layer interconnection structure whose occupied area of a contact part between top and bottom wiring patterns is suppressed and whose reliability is improved and provide the production for the semiconductor device.
CONSTITUTION: On a substrate 1, a first wiring layer 2 whose bottom plane is almost flat and is provided with a recessed part 5 on the surface is formed and an insulating layer 3 which covers the surface of the first wiring layer 2 is formed on the first wiring layer 2. The insulating layer 3 is provided with a through hole 4 and a second-wiring layer 6 is connected to the surface of the recessed part 5 of the first wiring layer 2 through the through hole 4. As for the production of the semiconductor device, the recessed part 5 is formed by etching after etching the through hole 4.



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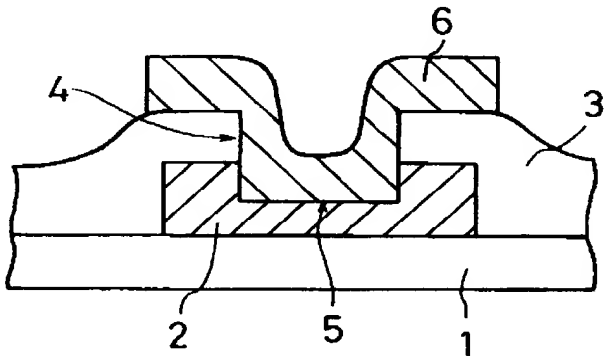
(54)【発明の名称】　半導体装置とその製造方法

(57)【要約】
【目的】　本発明は、半導体装置とその製造方法に関し、半導体装置の多層配線構造において、上下配線パターン間のコンタクト部の占有面積を抑え、かつ信頼性を向上した半導体装置とその製造方法を提供することを目的とする。
【構成】　本発明の半導体装置においては、基板上に、底面がほぼ平坦で表面に凹部を設けた第１の配線層が形成されており、その上に、第１の配線層の表面を覆う絶縁層が形成されている。絶縁層には、貫通孔が設けられ、第２の配線層が貫通孔を通って第１の配線層の凹部の表面と接続している。そして本発明の半導体装置の製造方法においては、貫通孔のエッチングに続いて凹部の形成がエッチングにより行われる。

原理説明図



１：基板　　４：貫通孔
２：第１の配線層　　５：凹部
３：（層間）絶縁層　　６：第２の配線層

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【特許請求の範囲】

【請求項1】　基板（1）上に形成され、底面がほぼ平坦で表面に凹部（5）を設けた第1の配線層（2）と、前記第1の配線層（2）の表面を覆う絶縁層（3）と、前記絶縁層（3）を貫通する貫通孔（4）と、
前記貫通孔（4）を通って前記第1の配線層（2）の前記凹部（5）の表面と接触する第2の配線層（6）とを有する半導体装置。

【請求項2】　前記凹部（5）の表面は、底面と、該底面に対して傾斜した面とを含む請求項1記載の半導体装置。

【請求項3】　基板（1）上に第1の配線層（2）を形成する工程と、
前記第1の配線層（2）を覆う絶縁層（3）を形成する工程と、
前記絶縁層（3）を貫通する貫通孔（4）と、前記第1の配線層（2）の一部表面（5）とをエッチングするエッチング工程と、
前記貫通孔（4）を通り、前記凹部（5）の表面と接触するように前記絶縁層（3）上に第2の配線層（6）を形成する工程とを有する半導体装置の製造方法。

【発明の詳細な説明】

【0001】

【産業上の利用分野】本発明は、半導体装置及び、その製造方法に関する。詳しくは、半導体装置においては、絶縁層を挟んで多層配線される配線間の接続技術に関する。

【0002】

【従来の技術】多層配線技術は集積回路における配線を多層化して、回路素子を効率的に集積化するもので、近年の半導体装置の微細化および高集積度化に伴い重要な技術となってきている。

【0003】多層配線構造においては、異なる配線間の電気的絶縁を確保するために層間絶縁膜が設けられる。そして、上下の配線間の電気的接続を得るために、この層間絶縁膜に貫通孔（コンタクトホール）を設け、この貫通孔を通して上下の配線パターン同士を接続させている。

【0004】この貫通孔における層間接続で重要なことは、上の配線層の貫通孔でのカバレッジと、上下配線層間の接続部の信頼性である。図6～図8に、従来技術による多層配線構造における上下配線パターンの接続のプロセスフローを示す。

【0005】図6において、表面に絶縁層を形成した基板20の上にAl（アルミニウム）、W（タングステン）等の第1層目の配線パターン21を形成し、その上に層間絶縁層22を形成し、さらにその上に、開口パターン23を有するレジストマスク層24を順次積層する。そしてフレオン系ガスによる等方性エッチングにより層間絶縁層22をエッチングして、図6に示すように

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断面がワインカットとなる開口部25を形成する。

【0006】次に、図7において、フレオン系ガスによる異方性エッチングによって、層間絶縁層22にさらにコンタクトホール26を貫通させ、第1層目の配線パターン21の表面を露出させる。この際、ワインカット形状の開口部25の深さ寸法l_1とコンタクトホール26の深さ寸法l_2とは、たとえば5：5あるいは6：4という一定の比になるように調整される。

【0007】次に、図8において、レジストマスク層24を除去した後、Al等の第2層目の配線パターン27を形成する。第1層目の配線パターン21と第2層目の配線パターン27とはコンタクトホール26を介して接続される。ワインカット形状の開口部25の存在により、コンタクト部の空着性、信頼性が向上する。

【0008】

【発明が解決しようとする課題】上述した従来の技術においては、等方性エッチングによって層間絶縁層22をワインカット形状にエッチングして開口部分を大きく広げて傾斜をつけたために、第2層目配線パターン27のカバレッジや接着力は確保されたが、コンタクトホール26の開口寸法よりも、その上のワインカット開口部25の開口寸法の方が大きくなってしまった。

【0009】このことは、例えばレジストパターンを0．8μmで設計したとしても、実際にできるコンタクトホールの開口パターンがたとえば1．5μm程度に広がってしまい高集積度化の障害となる。

【0010】従って、64MDRAMの場合のように、配線幅が狭くなり、配線密度が高くなると、コンタクトホール形成時に接着力、信頼性改善のための等方性エッチングをおこなう寸法的な余裕がなくなる。無理にコンタクトを形成すれば、接着力不足が生じたり、コンタクト不良を生じることになる。

【0011】これらを防止するためには、第1層目と第2層目の配線のコンタクト部の幅を大きくせざるを得なくなるために、高密度化に対して制限を加えてしまうというような問題があった。

【0012】本発明の目的は、半導体装置の多層配線構造において、上下配線パターン間のコンタクト部の占有面積を抑え、かつ信頼性を向上した半導体装置とその製造方法を提供することにある。

【0013】

【課題を解決するための手段】本発明の半導体装置においては、第1の配線層に凹部を設けて接続部とし、第2の配線層がその第1の配線層の凹部に入り込んで両者が接続される。このようにすることによって、第1の配線層と第2の配線層とのコンタクト面積を拡大し、接続部の信頼性を向上させる。

【0014】また、本発明の半導体装置の製造方法においては、上記凹部を形成するように第1層目の配線層にもエッチングを行なう。図1に、本発明の原理説明図を

示す。図は、半導体装置の断面の基本的な構造を示す。

【0015】必要に応じて層間絶縁膜を設けた基板1上に、底面がほぼ平坦で表面に凹部5を設けた第1の配線層2が形成されており、その上に、第1の配線層2の表面を覆う絶縁層3が形成されている。絶縁層3には、凹部5と整合した貫通孔4が設けられ、第2の配線層6が貫通孔4を通って第1の配線層2の凹部5の表面と接続している。

【0016】絶縁層3に貫通孔4をエッチングした後、第1の配線層2の表面もエッチングして凹部5を形成する。

【0017】

【作用】第1の配線層に凹部を設けたことにより、従来の技術よりもコンタクトホールにおける第1の配線層を第2の配線層とのコンタクト面積が増大する。このため、両配線層の接続が確実となり欠陥が減少する。ワインカット形状の開口部の省略により占有面積を節約でき、高集積化に寄与する。

【0018】

【実施例】図2～図4を参照して、本発明の実施例による半導体装置の製造方法のを説明する。なお、図2～図4において、半導体基板内に形成されるデバイス構造は、図示を省略する。また、その他のデバイス層や配線層があってもよい。

【0019】図2において、半導体基板1上に7000Å～1μmの厚みのPSG（リンガラス）による絶縁層11が形成され、その上に、Al合金あるいはW合金による第1の配線層2を形成する。この第1配線層2のAl合金材料としては、Al－Si（Si1%含有）、Al－Cu（Cu2%あるいは0．1%含有）、Ti－Al、Ti－TiN－Al、Ti－TiW－Al、Al－Ti－Cu（Cu0．1%含有）等が使用できる。

【0020】第1の配線層2の厚みは、その下に形成されるデバイスの種類によるが、例えばMOSトランジスタの場合には約5000Å厚で形成し、バイポーラトランジスタの場合には約1μmの厚みで形成される。

【0021】さらに、第1の配線層2の上に絶縁層11と同じくPSGにより第1の配線層11と同じ程度の厚みの層間絶縁層3を形成し、さらにその上に、レジストマスク層8を約0．5～2μmの厚みで順次積層する。このレジストマスク層8に、0．5～0．8μm径の開口パターン7を形成する。

【0022】このレジストマスク層8をエッチングマスクとして用い、フレオン系ガスによる異方性エッチングにより層間絶縁層3をエッチングして開口パターン7とほぼ同一径のコンタクトホール9をあけ、第1の配線層2を露出させる。この異方性エッチングは、反応性イオンエッチング（RIE）を使用し、たとえば0．2Torrに減圧した低真空中にCF_4とCHF3を1：1のモル比で混合したエッチングガスを供給し、RF出力450～500W程度で高周波放電して行う。

【0023】次に、図3において、第1の配線層2の表面に凹部5を形成する。凹部5の形成はRIEまたは電子サイクロトロン共鳴エッチング（ECR）を使用する。エッチングガスとしてのCl_2とデポジションガスとしてのBCl3やSiCl4の混合ガスを用い、エッチングガスとデポジションガスの比を変えることにより、エッチングされる領域の形状を制御する。

【0024】ほぼ垂直な側壁を形成する時は、エッチングガスとデポジションガスの比を、たとえば6：4位にしてエッチングする。側壁を傾斜させる時は、デポジションガスの比を増加させる。たとえば、エッチングガスとデポジションガスの比を（3以下）：（7以上）とする。

【0025】たとえば、Cl_2とBCl3の混合ガスの場合、Cl_2の含有率を10～20%と少なくする。SiCl4、BCl3等のデポジションガスを多めにすると、側面方向のエッチング速度を抑制したコントロールエッチングが行なわれ、傾斜した側面が得られる。

【0026】凹部5の深さはレーザEPD（End Point Detector）により、エッチング量をモニターしながら制御して、第1の配線層2の厚さの1／4～1／3程度とする。たとえば、約1500Åの深さを削り込む。

【0027】凹部5の傾斜は、Cl_2とBCl3の混合ガスでCl_2の含有率を10～20%とした時、配線材料がAl－Siの場合、垂直線に対し約30～45°となった。Al－Cuの場合にはさらに大きな角度となり底面に対してなだらかな裾野の傾斜を作った。

【0028】次に、レジスト層8を除去した後、イオンミリングあるいは高周波放電により、コンタクトホール9ないし凹部5の表面に付着した不要なデポジションガス等の膜を除去する。そして、その上に第2の配線層6を形成する。

【0029】第2の電極層6は、Al－Si合金、Ti／Al－Cu（0．1～2%）合金あるいはTi／Al－Si（1%）合金あるいはW合金等をスパッタあるいはCVD等により成長形成した後、配線パターンに従ったホトリソグラフィでパターニングする。

【0030】第2の配線層6の厚みは、バイポーラトランジスタの場合、たとえば約8000Å程度である。MOSトランジスタの場合は約5000Å程度である。Al合金に代えてW合金を使う場合も同様の厚さである。

【0031】なお、上記実施例で凹部5に傾斜面を形成する場合を説明したが、これは凹部5による接触面積拡大の他に、傾斜部としたことにより、スパッタにより第2の配線層を形成する場合、材料がよりよく付着して成長しやすくなりカバレッジを向上する。

【0032】もちろん、CVDで配線層を形成する場合等、図1のように凹部5の側面を垂直にしても、接触面

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積の拡大による信頼性向上の効果が得られる。垂直面と傾斜面を組み合わせてもよいことは言うまでもない。

【００３３】次に、図５に、本発明の他の実施例による半導体装置の断面構造を示す。これは、ＥＳＰＥＲ（Ｅｍｉｔｔｅｒ　Ｓｅｌｆ－ａｌｉｇｎｅｄ　ｗｉｔｈ　Ｐｏｌｙ－ｓｉｌｉｃｏｎ　Ｅｌｅｃｔｒｏｄｅ　Ｒｅｓｉｓｔｅｒ）等に適用できる例である。なお、図５ではデバイス部分は図示を省略してある。

【００３４】図５において、第１層目のＰＳＧ絶縁層１１の上にＡｌ合金による第１の電極パターン１０（これらは、それぞれ図示しないトランジスタのエミッタ、ベース、コレクタにそれぞれ接続されていると考えてよい）が形成され、その表面には先の実施例と同様な凹部が設けられている。さらに第２層目のＰＳＧ層１２と平坦化のための第３層目のＰＳＧ層１３が順次積層されている。

【００３５】なお、第１の電極層１１の間にある層１４は平坦化のための樹脂層である。そして、第３のＰＳＧ層１３にはコンタクトホール１５が形成されて、そこにＡｌ合金による第２の配線層１６が形成されている。

【００３６】以上実施例に沿って本発明を説明したが、本発明はこれらに制限されるものではない。たとえば、種々の変更、改良、組み合わせ等が可能なことは当業者に自明であろう。

【００３７】

【発明の効果】以上説明したように、本発明によれば、第１層目の配線層に凹部を設けて接続部とし、第２層目の配線層がその第１層目の配線層の凹部に入り込んで両者が接続されるようにすることによって、接触面積の増

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大により第２層目の配線層の信頼性を向上させることができ、コンタクト部作成に必要な面積の減少により半導体装置の高密度化を促進する。

【図面の簡単な説明】

【図１】本発明の原理を説明するための、半導体装置の断面の基本構造を示す図である。

【図２】本発明の実施例による半導体装置の製造方法の工程を示す断面図である。

【図３】図２の工程に続く工程を示す断面図である。

【図４】図３の工程に続く工程を示す断面図である。

【図５】本発明の他の実施例による半導体装置の断面図である。

【図６】従来の技術による半導体装置の製造方法の工程を示す断面図である。

【図７】図６の工程に続く工程を示す断面図である。

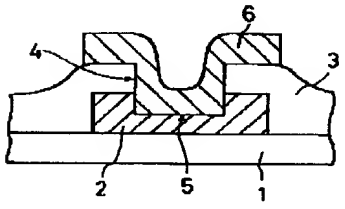
【図８】図７の工程に続く工程を示す断面図である。

【符号の説明】

１　基板
２　第１の配線層
３　絶縁層
４　貫通孔（コンタクトホール）
５　凹部
６　第２の配線層
７　開口パターン
８　レジストマスク層
９　コンタクトホール
１０　第１の電極パターン
１１　絶縁層
１６　第２の配線層

【図１】

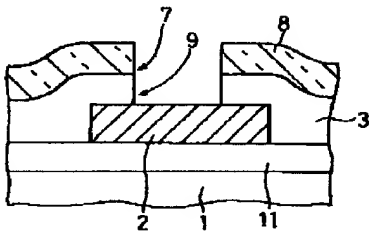
原理説明図



1：基板　4：貫通孔
2：第1の配線層　5：凹部
3：（層間）絶縁層　6：第2の配線層

【図２】

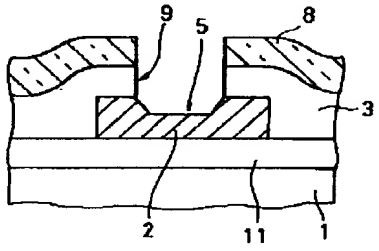
半導体装置の製造方法



7：開口パターン　9：コンタクトホール
8：レジストマスク層　11：絶縁層

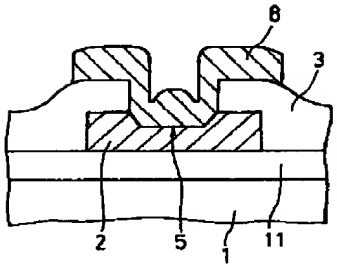
【図３】

半導体装置の製造方法



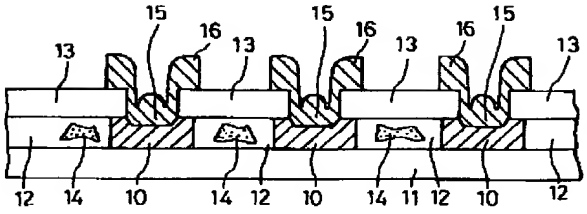
【図4】

半導体装置の製造方法



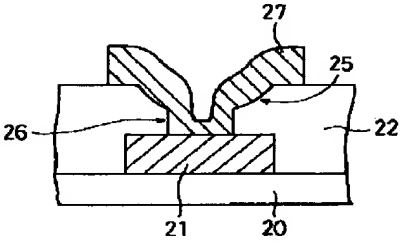
【図5】

ESPER型半導体装置



【図8】

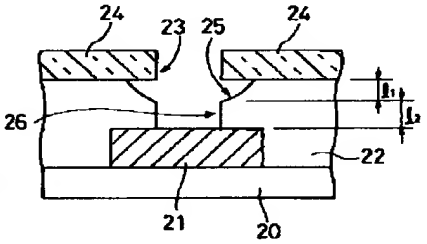
第2層目配線の形成（従来技術）



27：第2層目の配線パターン

【図7】

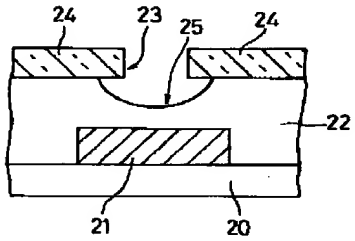
異方性エッチング（従来技術）



26：コンタクトホール

【図6】

等方性エッチング（従来技術）



20：基板
21：第1層目の配線パターン
22：層間絶縁膜
23：開口パターン
24：レジストマスク層
25：開口部

* NOTICES *

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] this invention relates to a semiconductor device and its manufacture technique. In detail, in a semiconductor device, it is related with the connection technique during the wiring by which a multilayer interconnection is carried out on both sides of an insulating layer.
[0002]
[Description of the Prior Art] Multilayer-interconnection technique multilayers the wiring in an integrated circuit, integrates a circuit element efficiently, and is important technique in connection with detailed-izing and high integration of a semiconductor device in recent years.
[0003] In multilayer-interconnection structure, in order to secure the electric insulation during a different wiring, a layer insulation layer is prepared. And in order to obtain the electrical installation during an up-and-down wiring, a breakthrough (contact hole) is prepared in this layer insulation layer, and up-and-down wiring patterns are connected to it through this breakthrough.
[0004] An important thing is the reliability of the coverage in the breakthrough of the upper wiring layer, and the connection between vertical wiring layers in the interlayer connection in this breakthrough. The process flow of connection of the vertical wiring pattern in the multilayer-interconnection structure by the conventional technique is shown in drawing 6 - view 8 .
[0005] In drawing 6 , the wiring patterns 21 of the 1st layer, such as aluminum (aluminum) and W (tungsten), are formed on the substrate 20 in which the insulating layer was formed on the front face, the layer insulation layer 22 is formed on it, and the laminating of the resist mask layer 24 which has the opening pattern 23 on it further is carried out one by one. And the layer insulation layer 22 is etched by the isotropic etching by Freon system gas, and as shown in drawing 6 , a cross section forms the opening 25 used as a wine cut.
[0006] Next, in drawing 7 , by the anisotropic etching by Freon system gas, the layer insulation layer 22 is made to penetrate the contact hole 26 further, and the front face of the wiring pattern 21 of the 1st layer is exposed. In this case, depth dimension l1 of the opening 25 of a wine cut configuration Depth dimension l2 of the contact hole 26 For example, it is adjusted so that it may become a fixed ratio called 5:5 or 6:4.
[0007] Next, in drawing 8 , after removing the resist mask layer 24, the wiring patterns 27 of the 2nd layer, such as aluminum, are formed. The wiring pattern 21 of the 1st layer and the wiring pattern 27 of the 2nd layer are connected through the contact hole 26. The ****** of the contact section and a reliability improve by presence of the opening 25 of a wine cut configuration.
[0008]
[Problem(s) to be Solved by the Invention] In the proior art mentioned above, since the layer insulation layer 22 was etched into the wine cut configuration, a part for opening was extended greatly and the inclination was attached by isotropic etching, although the coverage and the adhesive power of the 2nd-layer wiring pattern 27 were secured, the opening dimension of the wine cut opening 25 on it becomes large rather than the opening dimension of the contact hole 26.
[0009] The opening pattern of the contact hole actually made though for example, a resist pattern is designed by 0.8 micrometers spreads in about 1.5 micrometers, and this serves as the failure of high integration.
[0010] Therefore, if wiring width of face becomes narrow and a wiring density becomes high like [in the case of 64MDRAM], dimensional additional coverage to perform isotropic etching for adhesive power and a reliability improvement at the time of contact hole formation will be lost. If a contact is formed by force, the shortage of adhesive power will arise or a poor contact will be produced.
[0011] Since it could not but come to enlarge width of face of the contact section of the 1st layer and the 2nd-layer wiring in order to prevent these, there was a problem which is referred to as adding a limit to high-density-izing.
[0012] It is in the purpose of this invention offering the semiconductor device which stopped the occupancy area of the contact section between vertical wiring patterns, and improved the reliability in the multilayer-interconnection structure of a semiconductor device, and its manufacture technique.
[0013]
[Means for Solving the Problem] In the semiconductor device of this invention, a concavity is prepared in the 1st wiring layer, it considers as a connection, the 2nd wiring layer enters into the concavity of the 1st wiring layer, and both are connected. By doing in this way, the contact area of the 1st wiring layer and the 2nd wiring layer is expanded, and the reliability of a connection is

raised.
[0014] Moreover, in the manufacture technique of the semiconductor device of this invention, etching is performed also in a layer [1st] wiring layer so that the above-mentioned concavity may be formed. Principle explanatory drawing of this invention is shown in drawing 1 . Drawing shows the fundamental structure of the cross section of a semiconductor device.
[0015] On the substrate 1 which prepared the layer insulation layer if needed, a base is almost flat, the 1st wiring layer 2 which formed the concavity 5 is formed in the front face, and the wrap insulating layer 3 is formed in the front face of the 1st wiring layer 2 on it. The breakthrough 4 adjusted with the concavity 5 is formed in an insulating layer 3, and the 2nd wiring layer 6 has connected with the front face of the concavity 5 of the 1st wiring layer 2 through a breakthrough 4.
[0016] After etching a breakthrough 4 into an insulating layer 3, the front face of the 1st wiring layer 2 also etches, and a concavity 5 is formed.
[0017]
[Function] By having prepared the concavity in the 1st wiring layer, the contact area with the 2nd wiring layer increases the 1st wiring layer in a contact hole rather than a proior art. For this reason, connection of both the wirings layer becomes certain and a defect decreases. Ellipsis of opening of a wine cut configuration can save occupancy area, and it contributes to high integration.
[0018]
[Example] With reference to drawing 2 - view 4 , the manufacture technique's of the semiconductor device by the example of this invention is explained. In addition, in drawing 2 - view 4 , the device structure formed in a semiconductor substrate omits illustration. Moreover, there may be other device layers and wiring layers.
[0019] In drawing 2 , the insulating layer 11 by PSG (phosphorus glass) of 7000**-1micrometer thickness is formed on the semiconductor substrate 1, and the 1st wiring layer 2 by aluminum alloy or W alloy is formed on it. As a charge of aluminum alloy of this 1st wiring layer 2, aluminum-Si (Si1% inclusion), aluminum-Cu (Cu2% or 0.1% inclusion), Ti-aluminum, Ti-TiN-aluminum, Ti-TiW-aluminum, aluminum-Ti-Cu (Cu0.1% inclusion), etc. can be used.
[0020] Although the thickness of the 1st wiring layer 2 is based on the modality of device formed in the bottom of it, in the case of an MOS transistor, it is formed by abbreviation 5000** **, for example, and, in the case of a bipolar transistor, is formed by the thickness of about 1 micrometer.
[0021] Furthermore, the 1st wiring layer 11 and the layer insulation layer 3 of the thickness of the same grade are formed by PSG as well as an insulating layer 11 on the 1st wiring layer 2, and the laminating of the resist mask layer 8 is further carried out one by one by the thickness of about 0.5-2 micrometers on it. The opening pattern 7 of the diameter of 0.5-0.8 micrometer is formed in this resist mask layer 8.
[0022] The layer insulation layer 3 is etched by the anisotropic etching by Freon system gas, the contact hole 9 of the diameter of the same is mostly opened with the opening pattern 7, using this resist mask layer 8 as an etching mask, and the 1st wiring layer 2 is exposed. This anisotropic etching is CF4 in the low vacuum which used reactive ion etching (RIE), for example, was decompressed to 0.2Torrs. CHF3 The etching gas mixed by the mole ratio of 1:1 is supplied, and it carries out by carrying out a high frequency discharge by about [RF output 450-500W].
[0023] Next, a concavity 5 is formed in the front face of the 1st wiring layer 2 in drawing 3 . Formation of a concavity 5 uses RIE or electron cyclotron resonance etching (efficient consumer response). Cl2 as etching gas BCl3 as deposition gas SiCl4 The configuration of a field where it is etched is controlled by changing the ratio of etching gas and deposition gas using mixed gas.
[0024] When forming an almost perpendicular side attachment wall, the ratio of etching gas and deposition gas is made into the 6:4th place, and it etches. When making a side attachment wall incline, the ratio of deposition gas is made to increase. For example, the ratio of etching gas and deposition gas is made into : (3 or less) (7 or more).
[0025] For example, Cl2 BCl3 In the case of mixed gas, it is Cl2. Content is lessened with 10 - 20%. SiCl4 and BCl3 If the deposition gas of a grade is made [more], control etching which suppressed the etch rate of the orientation of the side face will be performed, and the inclined side face will be acquired.
[0026] The depth of a concavity 5 is controlled by laser EPD (End Point Detector), acting as the monitor of the amount of etching, and is made into about 1 of the thickness of the 1st wiring layer 2 / four to 1/3 with it. For example, the depth of about 1500 ** is deleted.
[0027] The inclination of a concavity 5 is Cl2. BCl3 It is Cl2 at mixed gas. When content was made into 10 - 20% and a wiring material was aluminum-Si, it became about 30-45 degrees to the vertical line. In aluminum-Cu, it became the still big angle, and the inclination of gently-sloping Susono was made to the base.
[0028] Next, after removing the resist layer 8, ion milling or a high frequency discharge removes the layers adhering to the contact hole 9 or the front face of a concavity 5, such as unnecessary deposition gas. And the 2nd wiring layer 6 is formed on it.
[0029] After the 2nd electrode layer 6 carries out growth formation of an aluminum-Si alloy, Ti / aluminum-Cu (0.1 - 2%) alloy, Ti / aluminum-Si (1%) alloy, or the W alloy by the spatter or CVD, patterning of it is carried out with the phot lithography according to the wiring pattern.
[0030] The thickness of the 2nd wiring layer 6 is in the case of a bipolar transistor, for example, an abbreviation 8000** grade. In the case of an MOS transistor, it is an abbreviation 5000** grade. It is the same thickness, when it replaces with aluminum alloy and it uses W alloy.
[0031] In addition, although the case where an inclined plane was formed in a concavity 5 in the above-mentioned example was explained, when forming the 2nd wiring layer by the spatter by having considered as the ramp other than the touch-area expansion by the concavity 5, a material adheres better, and this becomes easy to grow, and improves coverage.

[0032] Of course, when forming a wiring layer by CVD, as shown in drawing 1 , even if it makes the side face of a concavity 5 perpendicular, the effect of the enhancement in a reliability by expansion of a touch area is acquired. It cannot be overemphasized that a perpendicular and an inclined plane may be combined.
[0033] Next, the cross-section structure of the semiconductor device by other examples of this invention is shown in drawing 5 . This is an example applicable to ESPER (Emitter Self-aligned with Poly-silicon Electrode Resister) etc. In addition, in drawing 5 , the device fraction has omitted illustration.
[0034] In drawing 5 , the 1st electrode pattern 10 (you may think that these are connected to the emitter of the transistor which is not illustrated, respectively, the base, and a collector, respectively) by aluminum alloy is formed on the PSG insulating layer 11 of the 1st layer, and the same concavity as a previous example is prepared in the front face. Furthermore, the laminating of the layer 2nd] PSG layer 12 and the layer [3rd] PSG layer 13 for a flattening is carried out one by one.
[0035] In addition, the layer 14 between the 1st electrode layer 11 is a resin layer for a flattening. And the contact hole 15 is formed in the 3rd PSG layer 13, and the 2nd wiring layer 16 by aluminum alloy is formed there.
[0036] Although this invention was explained in accordance with the example above, this invention is not restricted to these. for example, various change, enhancement, combination, etc. are possible -- this contractor -- obvious -- it will be .
[0037]
[Effect of the Invention] According to this invention, as explained above, a concavity is prepared in a layer [1st] wiring layer, it considers as a connection, and a layer [2nd] wiring layer enters into the concavity of the layer [1st] wiring layer, by connecting both, the reliability of a layer [2nd] wiring layer can be raised by increase of a touch area, and high-density-ization of a semiconductor device is promoted by decrement of an area required for a contact section creation.

[Translation done.]

* NOTICES *

Effect

[Effect of the Invention] According to this invention, as explained above, a concavity is prepared in a layer [1st] wiring layer, it considers as a connection, and a layer [2nd] wiring layer enters into the concavity of the layer [1st] wiring layer, by connecting both, the reliability of a layer [2nd] wiring layer can be raised by increase of a touch area, and high-density-ization of a semiconductor device is promoted by decrement of an area required for a contact section creation.

[Translation done.]

* NOTICES *

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] In the proior art mentioned above, since the layer insulation layer 22 was etched into the wine cut configuration, a part for opening was extended greatly and the inclination was attached by isotropic etching, although the coverage and the adhesive power of the 2nd-layer wiring pattern 27 were secured, the opening dimension of the wine cut opening 25 on it becomes large rather than the opening dimension of the contact hole 26.
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[Translation done.]

* NOTICES *

MEANS

[Means for Solving the Problem] In the semiconductor device of this invention, a concavity is prepared in the 1st wiring layer, it considers as a connection, the 2nd wiring layer enters into the concavity of the 1st wiring layer, and both are connected. By doing in this way, the contact area of the 1st wiring layer and the 2nd wiring layer is expanded, and the reliability of a connection is raised.
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[Translation done.]

* NOTICES *

OPERATION

[Function] By having prepared the concavity in the 1st wiring layer, the contact area with the 2nd wiring layer increases the 1st wiring layer in a contact hole rather than a proior art. For this reason, connection of both the wirings layer becomes certain and a defect decreases. Ellipsis of opening of a wine cut configuration can save occupancy area, and it contributes to high integration.

[Translation done.]

EXAMPLE

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